Claims

[c1] 1. A method for reading a non-volatile memory with multi-level output currents, the non-volatile memory comprising a plurality of multi-level memory cells having at least a first, a second, a third, and a fourth programming states, the method comprising:
applying a first reading voltage on a conductor of the memory cell;
applying a second reading voltage on a drain of the memory cell; and
grounding a source of the memory cell, thereby obtaining an output current;
wherein the output current comprises a maximum output current corresponding to the memory cell in the first programming state, a first output current corresponding to the memory cell in the second programming state, a second output current corresponding to the memory cell in the third programming state, and a third output current corresponding to the memory cell in the fourth programming state.

[c2] 2. The method of claim 1 wherein the maximum output current is larger than the first output current, which is larger than the second output current, which is larger than the third output current.

[c3] 3. The method of claim 1 wherein each memory cell comprises a source, a drain, a channel formed between the source and the drain, a first isolation layer formed on the channel, a non-conducting dielectric layer formed on the first isolation layer, a second isolation layer formed on the non-conducting dielectric layer and a conductor formed on the second isolation layer, the non-conducting dielectric layer comprising a first region nearby the drain and a second region nearby the source.

[c4] 4. The method of claim 3 wherein the first programming state represents that both the first region and the second region are not injected with electrons, the second programming state represents that the second region is not injected with electrons but the first region, the third programming state represents that the first region is not injected with electrons but the second region, and the fourth programming state represents that both the first region and the second region are injected with electrons.

[c5] 5. The method of claim 3, wherein the non-conducting dielectric layer comprises silicon nitride.

[c6] 6. The method of claim 3, wherein the first isolation layer and the second isolation layer both comprise silicon dioxide.

[c7] 7. The method of claim 3, wherein the conductor comprises polysilicon.